ABSTRACT OF THE DISCLOSURE

A data transfer controller is provided which can reduce a CPU control load necessary for data transfer cyclically using a plurality of data transfer areas. A DMAC constituting the data transfer controller is initially set with a transfer start address of a transfer source or transfer destination by a CPU, issues an interrupt to CPU each time the data transfer responding to a transfer request from the transfer source reaches a predetermined data amount based upon the transfer start address, and initializes an address of the transfer source or transfer destination to the transfer start address each time the interrupt is issued predetermined plural times. After CPU sets once the data transfer conditions to DMAC, CPU can continue data processing by repetitively using a limited number of memory areas, without performing any process of repetitively setting the data transfer conditions necessary for a data transfer control for receiving voice data.

09873242.060501